

display will be reduced. Further more the novel waveform totally gets rid of the black line effect during the frame change which incurred in the prior art display.

Thirdly, software embedded in the display controller is getting simpler in the present invention, and related memory is much smaller than that of the prior art.

Claims: I claim:

1. A localized driving means for a cholesteric liquid crystal display comprising:
 - a. an erasing pulse with its pulse configuration sufficiently activating display elements to an unstable planar state;
 - b. an addressing pulse with its pulse configuration sufficiently activating display elements to an unstable focal conic state;
 - c. a bias voltage pulse with its amplitude not less than a threshold voltage from planar to focal conic structure.

the erasing pulse and the addressing pulse, superimposed to the bias pulse, applied to a predetermined location in the same row and at the same time, whereby the unstable planar state and the unstable focal conic state are displayed simultaneously in at least a partial area of the display during the activating; whereby an stable planar state and an stable focal conic state are displayed simultaneously in at least a partial area of the display by the end of activating process.

2. The driving means according to claim 1 wherein the erasing pulse is a narrow pulse “ V_E ” with amplitude higher than the cholesteric to nematic phase change voltage.
3. The driving means according to claim 1 wherein the addressing pulse is a narrow pulse “ V_A ” with amplitude approximately equal to unstable focal conic state.
4. The driving means according to claim 1 wherein the bias voltage is a controllable voltage “ V_{NP} ” determining the unstable planar state.
5. The driving means according to claim 1 wherein the unstable planar state is a displayable optical “on” state.
6. The driving means according to claim 1 wherein the unstable focal conic state is a displayable optical “off” state.

7. The driving means according to claim 1 wherein the stable planar state is another displayable optical “on” state.
8. The driving means according to the claim 1 wherein the stable focal conic state is another displayable optical “off” state.
9. The driving means according to the claim 1 wherein at least a partial area addressing means is a whole frame addressing means.
10. The driving means according to claim 1 wherein the partial area means localized addressing means, which allows partial writing or changing the information content based on one pixel, one line or multiple lines, while the rest information contents are maintaining their originals in the display area.
11. The driving means according to claim 10 wherein the localized addressing is handwriting display mode.
12. The driving means according to claim 10 wherein the localized addressing is a typewriting display mode.
13. The driving means according to claim 10 wherein the localized addressing is partial correction display mode.
14. The driving means according to claim 10 wherein the localized addressing is a data input display mode.
15. The driving means according to claim 10 wherein the localized addressing is a word processing display mode.
16. A part of waveform generating circuit comprising:
 - a. a programmable resistor, R_x ;
 - b. a series fixed resistors R with approximately the same value;
 - c. a divider circuit with multiple outputs;
 - d. a DC pulse voltage source, V_{LCD} ;

The programmable resistor creates variable bias voltage wherein the highest R_x represents the lowest bias voltage and vice versa, whereby optimal localized addressing mode and whole frame addressing mode can be automatically or manually convertible.
17. The waveform generating circuit according to claim 16 wherein the multiple outputs are V_{NP} , $2V_{NP}$, V_A , V_A+V_{NP} and V_E .

18. The waveform generating circuit according to claim 16 wherein the waveform is governed by the following formulas

$$V_E = V_{LCD}$$

$$V_A = V_E - 2V_{NP}$$

$$V_{NP} \geq V_T.$$

19. The waveform generating circuit according to claim 16 wherein the waveform is coupled to at least one common "X" driver and to at least one segment "Y" driver to composite DC-free AC pulses, V_{NP} , V_A , and V_E .

20. The waveform generating circuit according to claim 19 wherein the V_{NP} , V_A , and V_E pulses are non-parasitical driving pulses.

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